FIG. 1

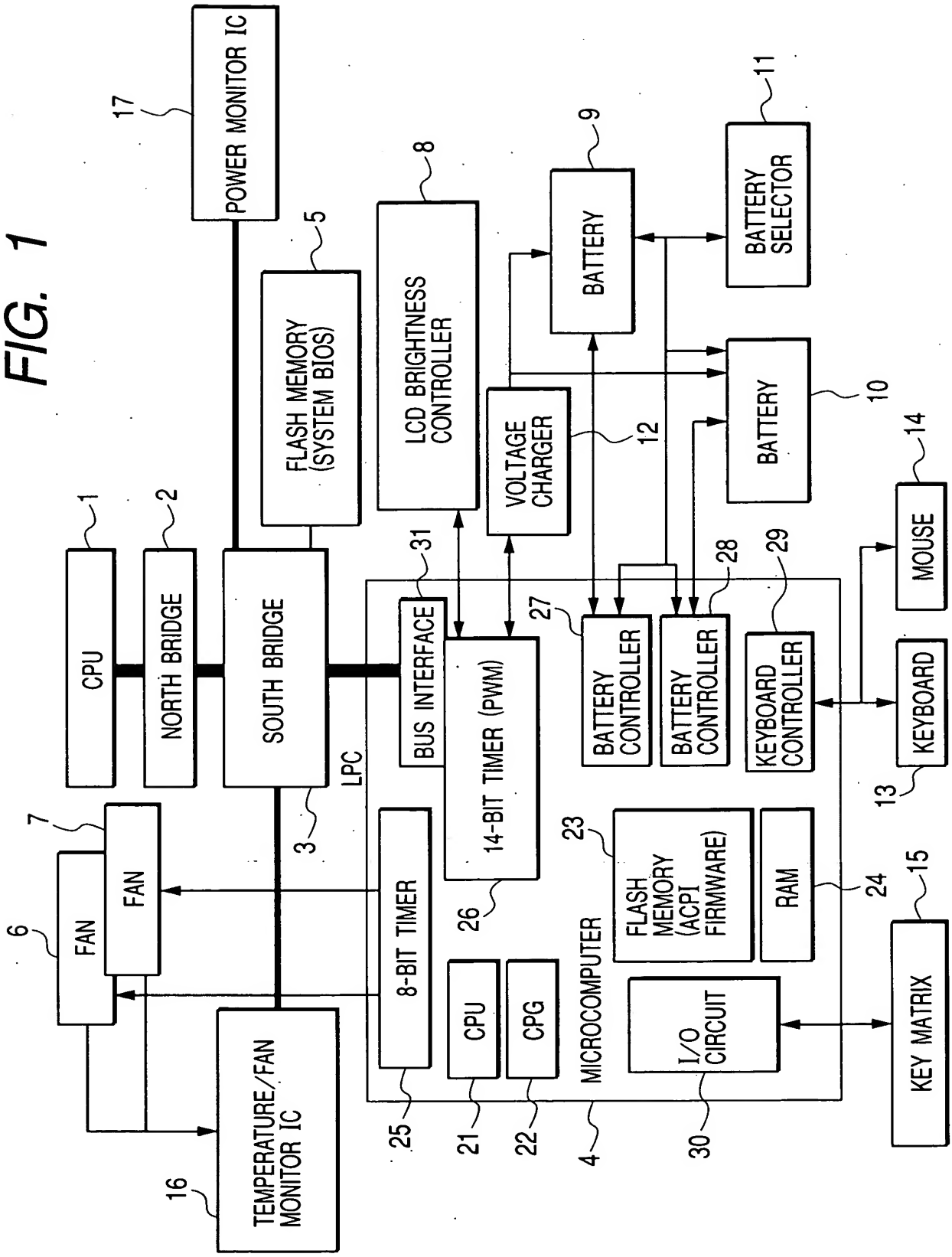
POWER MONITOR IC
17
FLASH MEMORY (SYSTEM BIOS)
5
LCD BRIGHTNESS CONTROLLER
8
BATTERY
9
BATTERY SELECTOR
11
CPU
1
NORTH BRIDGE
2
SOUTH BRIDGE
3
LPC
BUS INTERFACE
31
VOLTAGE CHARGER
12
BATTERY
10
MOUSE
14
FAN
7
FAN
6
8-BIT TIMER
14-BIT TIMER (PWM)
26
BATTERY CONTROLLER
27
BATTERY CONTROLLER
28
KEYBOARD CONTROLLER
29
KEYBOARD
13
TEMPERATURE/FAN MONITOR IC
16
CPU
21
CPG
22
MICROCOMPUTER
4
FLASH MEMORY (ACPI FIRMWARE)
23
RAM
24
I/O CIRCUIT
30
KEY MATRIX
15
25

FIG. 2

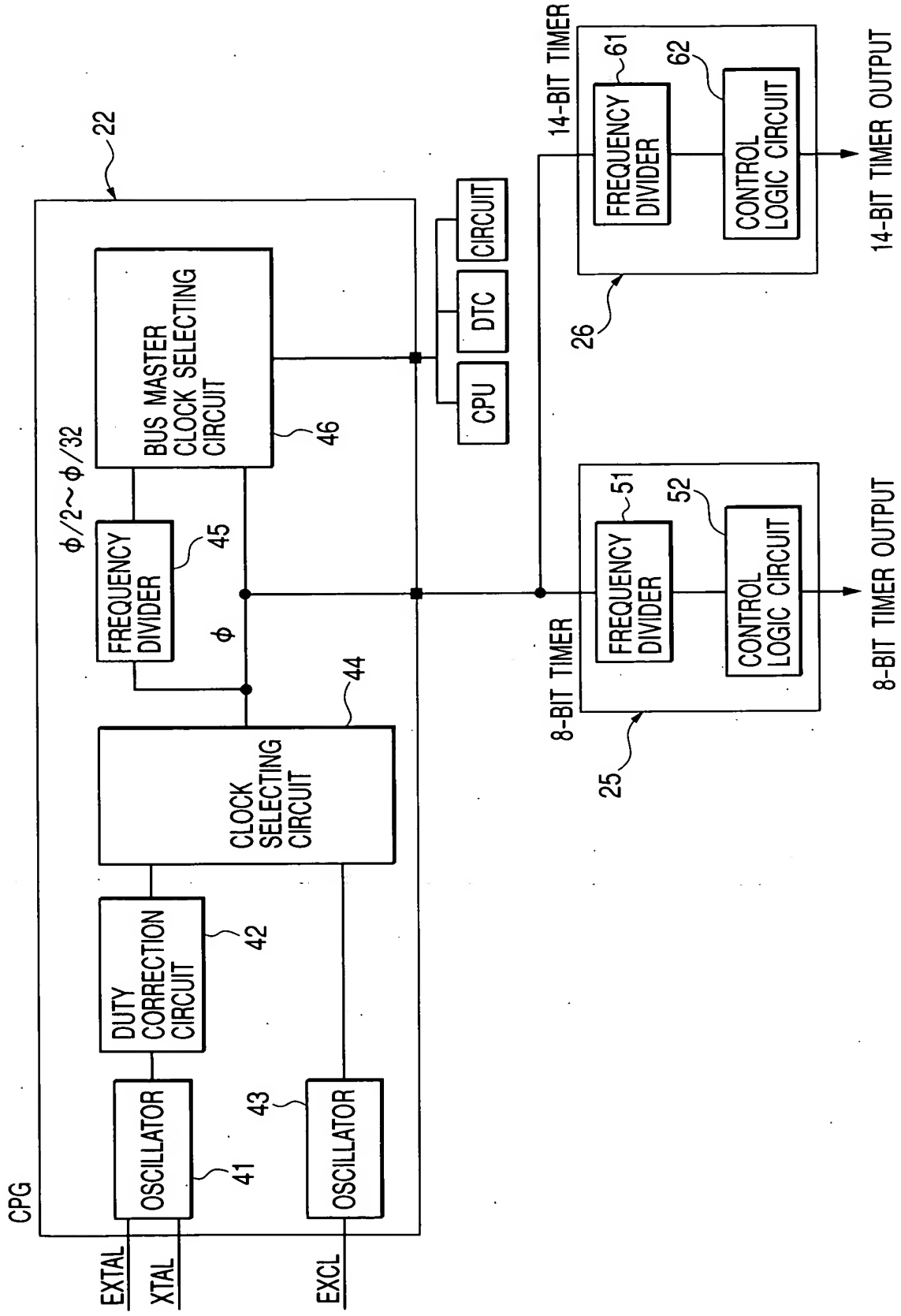
22
CPG
BUS MASTER CLOCK SELECTING CIRCUIT
46
FREQUENCY DIVIDER
45
φ/2~φ/32
φ
CLOCK SELECTING CIRCUIT
44
DUTY CORRECTION CIRCUIT
42
OSCILLATOR
41
43
OSCILLATOR
EXTAL
XTAL
EXCL
CPU
DTC
CIRCUIT
14-BIT TIMER
FREQUENCY DIVIDER
61
CONTROL LOGIC CIRCUIT
62
14-BIT TIMER OUTPUT
26
8-BIT TIMER
FREQUENCY DIVIDER
51
CONTROL LOGIC CIRCUIT
52
8-BIT TIMER OUTPUT
25

FIG. 3

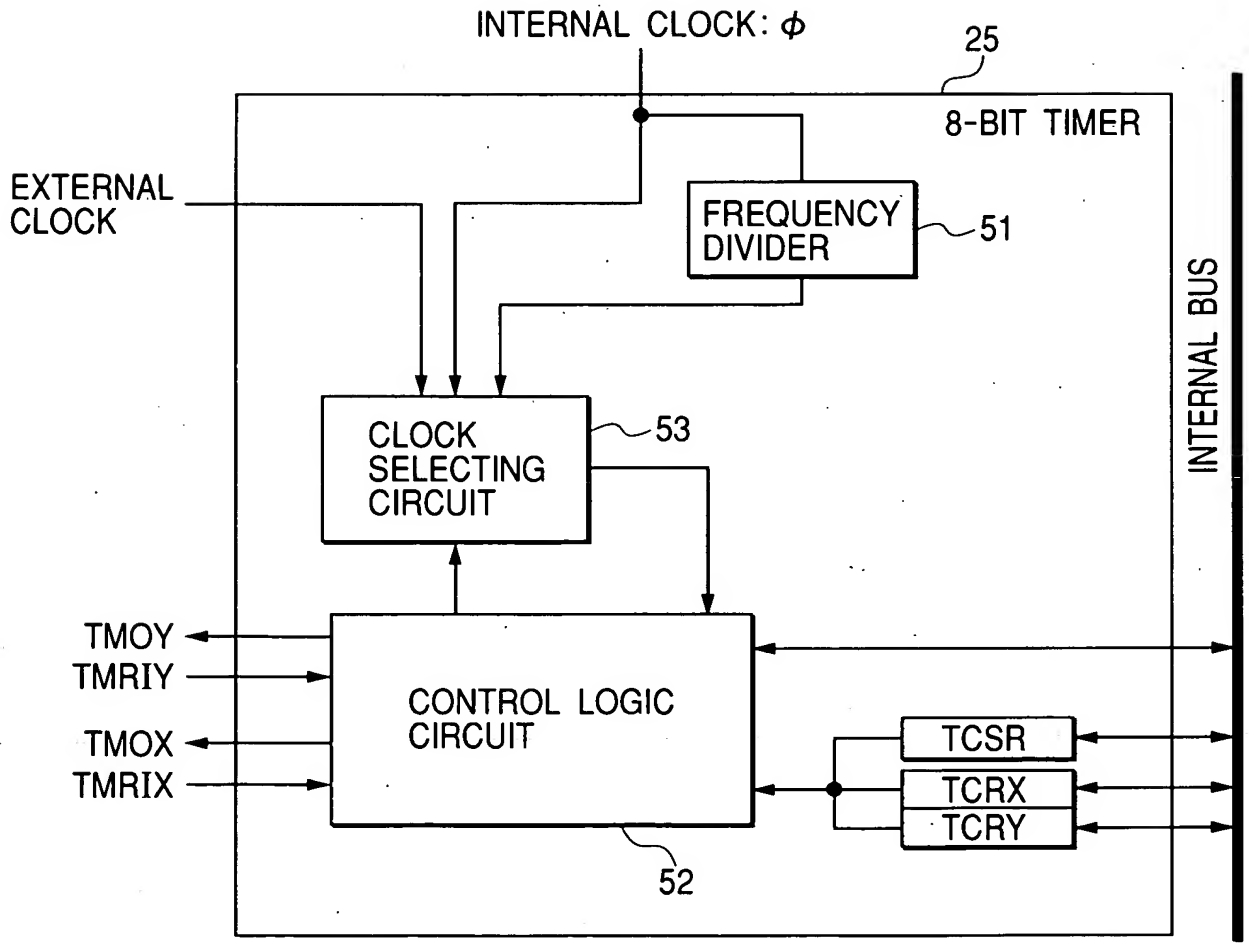
INTERNAL CLOCK: φ
25
8-BIT TIMER
EXTERNAL CLOCK
FREQUENCY DIVIDER
51
INTERNAL BUS
CLOCK SELECTING CIRCUIT
53
TMOY
TMRIY
TMOX
TMRIX
CONTROL LOGIC CIRCUIT
TCSR
TCRX
TCRY
52

FIG. 4

TCRX	TCSR			DESCRIPTION
BIT 5	BIT 2	BIT 1	BIT 0	
CKSX	CKS 2	CKS 1	CKS 0	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
1	0	0	0	CLOCK INPUT INHIBIT
1	0	0	1	COUNT IN ϕ/2,048
1	0	1	0	COUNT IN ϕ/4,096
1	0	1	1	COUNT IN ϕ/8,192
1	1	0	0	COUNT IN A COMPARE MATCH
—	1	0	1	
—	1	1	0	
—	1	1	1	

FIG. 5

TCRY	TCSR			DESCRIPTION
BIT 4	BIT 2	BIT 1	BIT 0	
CKSY	CKS 2	CKS 1	CKS 0	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
1	0	0	0	CLOCK INPUT INHIBIT
1	0	0	1	COUNT IN ϕ/4,096
1	0	1	0	COUNT IN ϕ/8,192
1	0	1	1	COUNT IN ϕ/16,384
1	1	0	0	COUNT IN AN OVERFLOW
—	1	0	1	
—	1	1	0	
—	1	1	1	

FIG. 6

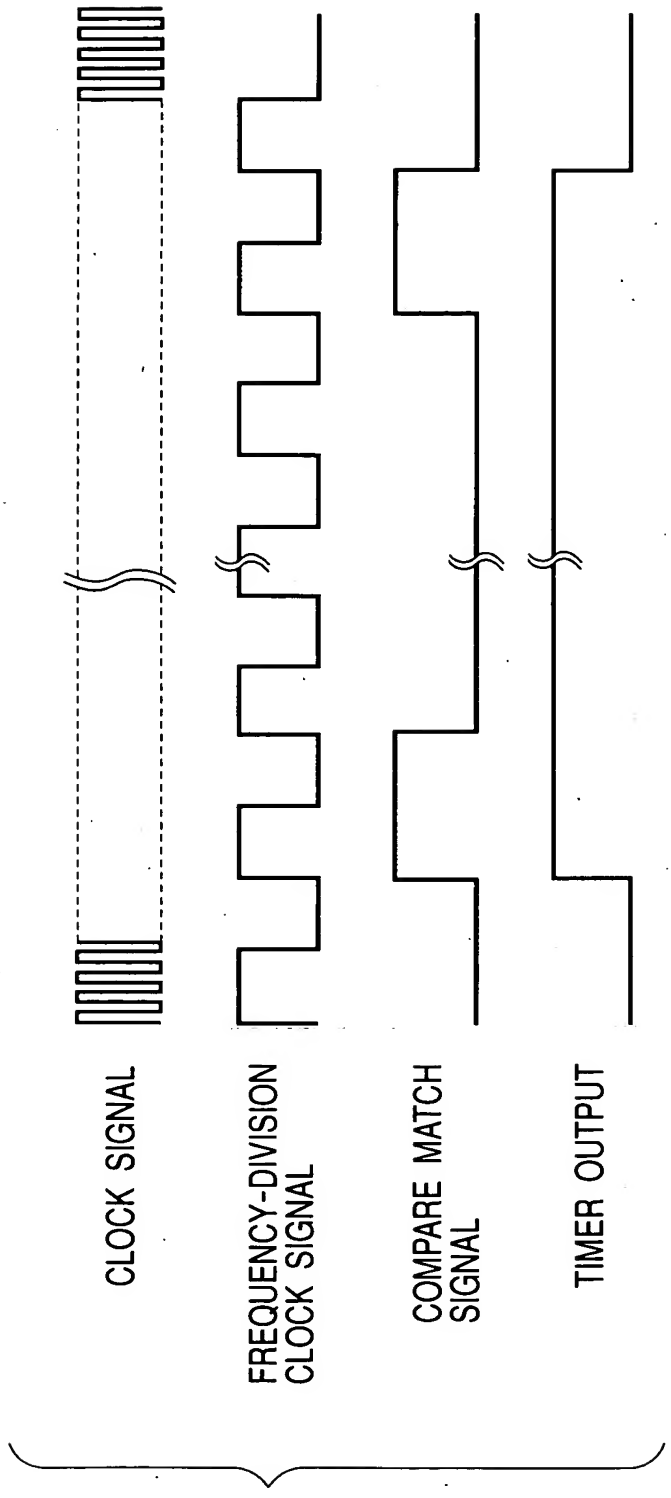
CLOCK SIGNAL
FREQUENCY-DIVISION CLOCK SIGNAL
COMPARE MATCH SIGNAL
TIMER OUTPUT

FIG. 7

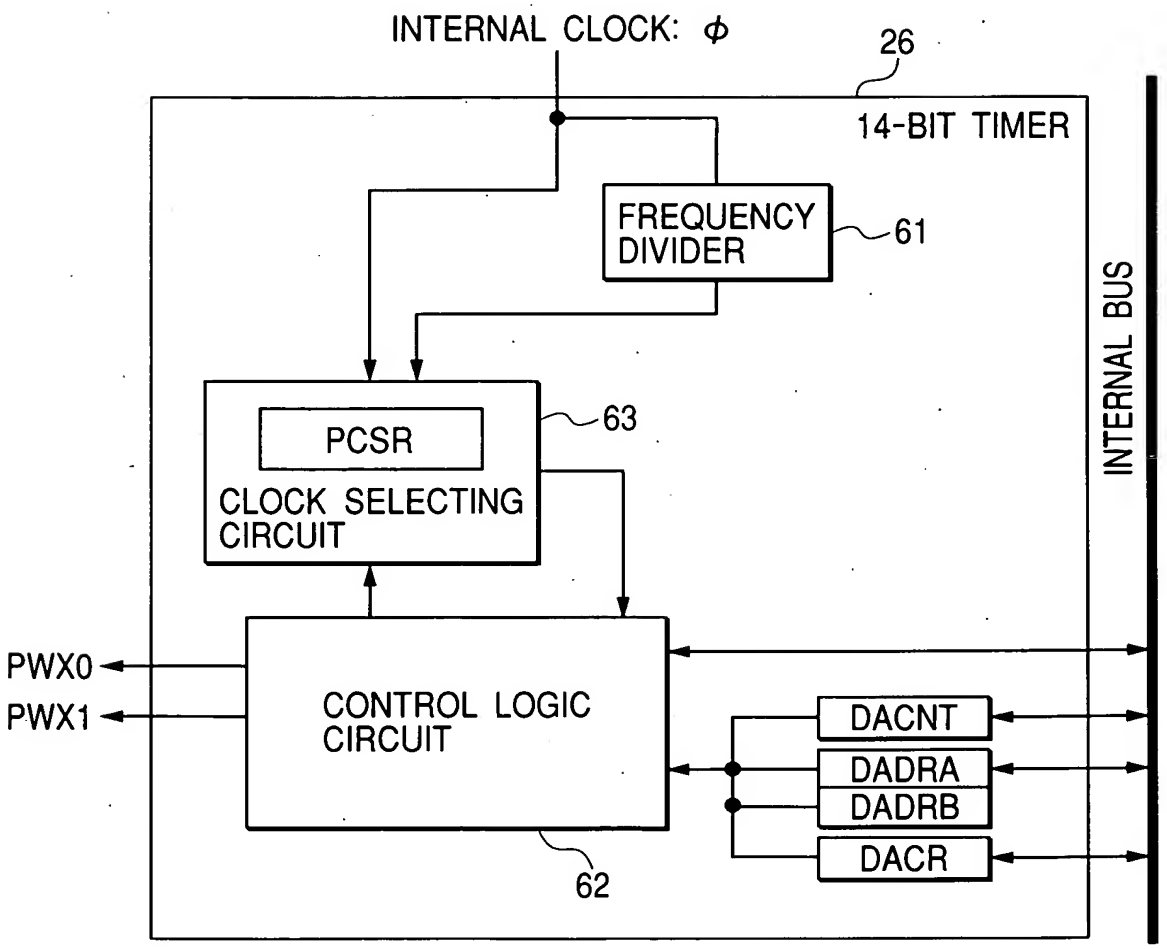
INTERNAL CLOCK: φ
26
14-BIT TIMER
FREQUENCY DIVIDER
61
INTERNAL BUS
PCSR
63
CLOCK SELECTING CIRCUIT
PWX0
PWX1
CONTROL LOGIC CIRCUIT
DACNT
DADRA
DADRB
DACR
62

FIG. 8

BIT	BIT NAME	INITIAL VALUE	R/W	DESCRIPTION
7 6	PWCKX1B PWCKX1A	0 0	R/W R/W	PWMX_1 CLOCK SELECT WHEN CKS OF DACR OF PWMX_1 IS 1, SELECTS A CLOCK (REFER TO FIG. 9)
5 4	PWCKX0B PWCKX0A	0 0	R/W R/W	PWMX_0 CLOCK SELECT WHEN CKS OF DACR OF PWMX_0 IS 1, SELECTS A CLOCK (REFER TO FIG. 9)
3	PWCKX1C	0	R/W	PWMX_1 CLOCK SELECT WHEN CKS OF DACR OF PWMX_1 IS 1, SELECTS A CLOCK (REFER TO FIG. 9)
2 1				
0	PWCKX0C	0	R/W	PWMX_0 CLOCK SELECT WHEN CKS OF DACR OF PWMX_0 IS 1, SELECTS A CLOCK (REFER TO FIG. 9)

FIG. 9

PWCKX0C PWCKX1C	PWCKX0B PWCKX1B	PWCKX0A PWCKX1A	RESOLUTION(T)
0	0	0	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 2
0	0	1	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 64
0	1	0	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 128
0	1	1	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 256
1	0	0	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 1,024
1	0	1	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 4,096
1	1	0	OPERATES AT A SYSTEM CLOCK CYCLE MULTIPLIED BY 16,384
1	1	1	SETTING INHIBIT

FIG. 10

BIT	BIT NAME	DESCRIPTION
15	DA13	OUTPUT WAVEFORM SETTING (REFER TO FIG. 11)
14	DA12	
13	DA11	
12	DA10	
11	DA9	
10	DA8	
9	DA7	
8	DA6	
7	DA5	
6	DA4	
5	DA3	
4	DA2	
3	DA1	
2	DA0	
1	CFS	·R/W CARRIER FREQUENCY SELECT 0: OPERATES AT BASIC CYCLE=RESOLUTION(T) MULTIPLIED BY 64 THE RANGE OF THE VALUES OF DA0 TO DA13 IS H'0100 TO H'3FFF 1: OPERATES AT BASIC CYCLE=RESOLUTION(T) MULTIPLIED BY 256 THE RANGE OF THE VALUES OF DA0 TO DA13 IS H'0040 TO H'3FFF
0	—	RESERVED BIT

FIG. 11

RESOLUTION T (μs)	CONVERSION CYCLE (μs)	DADRA,B (DA13~DA0)	LOW WIDTH (μs)	HIGH WIDTH (μs)
0.1	1638.4	H'0000	0.1	1638.3
		:	:	:
		:	:	:
		H'1000	409.6	1228.7
		:	:	:
		:	:	:
		H'3FFF	1638.3	0.1
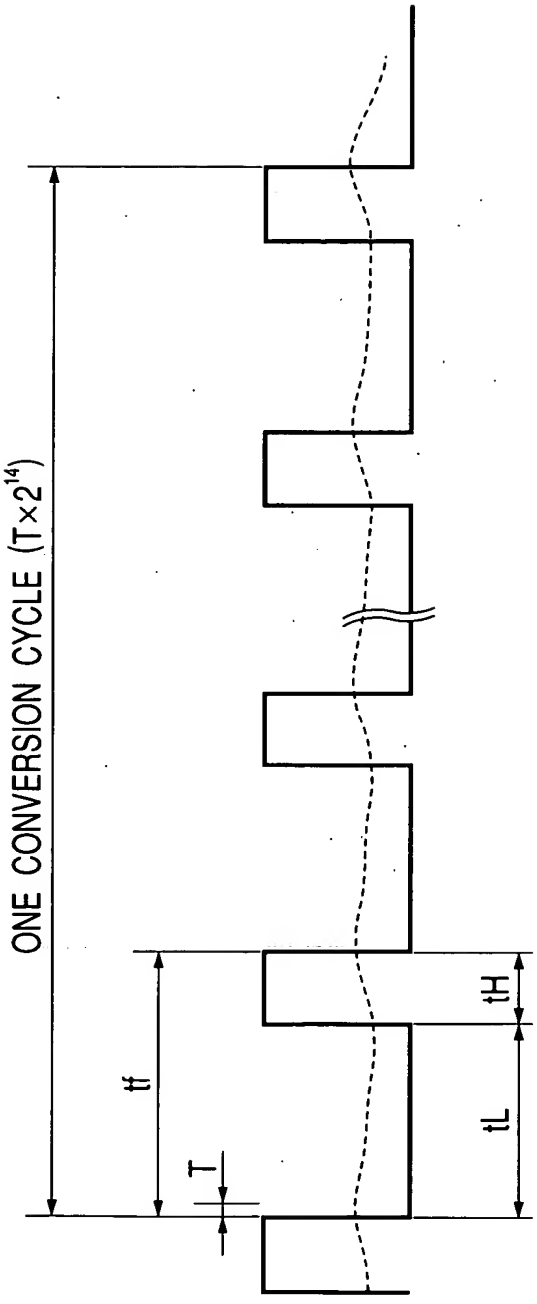
FIG. 12